REMARKS

The Office Action mailed January 17, 2007 has been carefully reviewed and the following remarks have been made in consequence thereof.

Claims 26-29 are now pending in this application. Claims 26, 28, and 29 have been rejected. Claim 27 is withdrawn. Claims 1-25 are canceled without prejudice, waiver, or disclaimer. No new matter has been added.

The rejection of Claim 26 under 35 U.S.C. § 103(a) as being unpatentable over Biard (U.S. Patent No. 4,661,726) ("Biard") is respectfully traversed.

Biard describes a buffered FET logic (BFL) gate. The BFL gate includes a plurality of transistors (32, 33, 36, and 37, Figure 4). The transistors (32, 33, and 36) are designed to have twice the width of the transistor (37) to provide equal positive and negative slew rates for charging a wiring capacitance on an output node. Notably, Biard describes a single output node (OUT).

Claim 26 recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an inverter stage input . . . an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output . . . a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel . . . a first output at a first electrical node between said voltage drop circuit and said first channel . . . and a second output at a second electrical node between said voltage drop circuit and said second channel, wherein said second electrical node comprises a redistribution point configured to recognize and transmit a first signal to a circuit other than said BFL level-shifting/inverter circuit, said first electrical node comprises a redistribution point configured to recognize and transmit a level-shifted signal to a circuit other than said BFL level-shifting/inverter circuit, and wherein the level-shifted signal is generated by shifting a voltage level of the first signal."

Biard does not describe or suggest a buffered field effect transistor logic (BFL) level-shifting/inverter circuit as recited in Claim 26. Specifically, Biard does not describe or suggest a first output at a first electrical node between a voltage drop circuit and the first channel, and a second output at a second electrical node between the voltage drop circuit and the second channel, where the second electrical node is a redistribution point configured to recognize and transmit a first signal to a circuit other than the BFL level-shifting/inverter circuit, the first electrical node is a redistribution point configured to recognize and transmit a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit. Rather, Biard describes a BFL gate including a single output node and a plurality of transistors including a first, a second, a third, and a fourth transistor. The first, second, and third transistors are designed to have twice a width of the fourth transistor to provide equal positive and negative slew rates for charging a wiring capacitance on an output node. Specifically, Biard does not describe nor suggest two electrical output nodes.

MPEP 2112, Section IV, states the following:

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic...
>
> To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.
>
> In relying on the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

The Office Action asserts on pages 4 and 5, respectively, that "the node between elements 32 and 33 **could** be used as an output" and "[a] node can function as an output and hence is an output." Thus, the Office Action appears to rely on the theory of inherency.

Applicant respectfully submits that a person of ordinary skill in the art should understand that, in network, a node is a redistribution point that transmits data. More

specifically, a person of ordinary skill in the art should understand that a node is configured to recognize and process or forward transmissions to other nodes. However, Biard does not describe or suggest the use of a second node between elements 32 and 33. As such, the Office Action does not support the allegation of inherency by providing a basis in fact and/or technical reasoning to support a combination of a second electrical node that is a redistribution point configured to recognize and transmit a first signal to a circuit other than a BFL level-shifting/inverter circuit and a first electrical node that is a redistribution point configured to recognize and transmit a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit.

Accordingly, for at least the reasons set forth above, Claim 26 is submitted to be patentable over Biard.

For at least the reasons set forth above, Applicant respectfully requests that the Section 103 rejection of Claim 26 be withdrawn.

The rejection of Claims 28 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Biard and further in view of Tohyama (U.S. Patent No. 4,810,907) ("Tohyama") and Alok et al. (U.S. Patent No. 6,559, 068) ("Alok") is respectfully traversed.

Biard is described above. Tohyama describes a level shift circuit. The circuit includes a plurality of metal semiconductor field effect transistors (MESFETs) (Q1 and Q2) with a resistor (R) between the MESFETs.

Alok describes a method for improving inversion layer mobility in a silicon carbide metal-oxide semiconductor field-effect transistor (MOSFET) is provided. The method includes positioning a silicon carbide substrate and metallic impurities in a chamber, and forming an oxide layer on a surface of the silicon carbide substrate by introducing a gaseous mixture of hydrogen and oxygen into the chamber.

Applicant respectfully submits that the Section 103 rejection of Claims 28 and 29 is not a proper rejection. As is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent

some teaching, suggestion, or incentive supporting the combination. None of Biard, Tohyama, nor Alok, considered alone or in combination, describe nor suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicant respectfully submits that it would not be obvious to one skilled in the art to combine Biard with Tohyama or Alok because there is no motivation to combine the references suggested in the cited art itself.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicant's disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejection is based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Since there is no teaching nor suggestion in the cited art for the combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicant requests that the Section 103 rejection of Claims 28 and 29 be withdrawn.

Claim 28 recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an inverter stage input . . . an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output . . . a buffered field effect transistor logic (BFL) stage responsive to said inverted output, said BFL stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a resistor electrically connected in series between said first channel and said second channel . . . a first output at a first electrical node between said resistor and said first channel . . . and a second output at a second electrical node between said resistor and said second channel, wherein said circuit is fabricated on a silicon carbide substrate, wherein said second electrical node comprises a redistribution point configured to recognize and transmit a first signal to a circuit other than said BFL level-shifting/inverter circuit, said first electrical node comprises a redistribution point configured to recognize and transmit a level-shifted signal to a circuit other than said BFL level-shifting/inverter circuit, and wherein the level-shifted signal is generated by shifting a voltage level of the first signal."

None of Biard, Tohyama, nor Alok, considered alone or in combination, describe or suggest a buffered field effect transistor logic (BFL) level-shifting/inverter circuit as recited in Claim 28. Specifically, none of Biard, Tohyama, nor Alok, considered alone or in combination, describe or suggest a first output at a first electrical node between a resistor and a first channel, and a second output at a second electrical node between the resistor and a second channel, where the second electrical node is a redistribution point configured to recognize and transmit a first signal to a circuit other than the BFL level-shifting/inverter circuit, the first electrical node is a redistribution point configured to recognize and transmit a level-shifted signal to a circuit other than the BFL level-shifting/inverter circuit. Rather, Biard describes a BFL gate including a single output node and a plurality of transistors including a first, a second, a third, and a fourth transistor. The first, second, and third transistors are designed to have twice a width of the fourth transistor to provide equal positive and negative slew rates for charging a wiring capacitance on an output node. Specifically, Biard does not describe nor suggest two electrical output nodes. Tohyama describes a

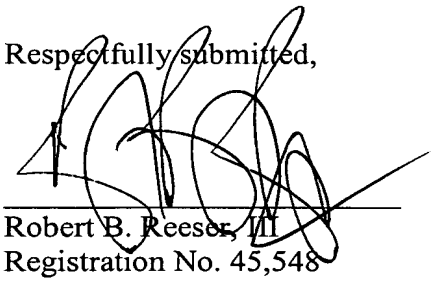
level shift circuit including a plurality of metal semiconductor field effect transistors (MESFETs) with a resistor between the MESFETs, and Alok describes a silicon carbide metal-oxide semiconductor field-effect transistor. Accordingly, for the reasons set forth above, Claim 28 is submitted to be patentable over Biard and further in view of Tohyama and Alok.

Claim 29 depends from independent Claim 28. When the recitations of Claim 29 are considered in combination with the recitations of Claim 28, Applicant submits that dependent Claim 29 likewise is patentable over Biard and further in view of Tohyama and Alok.

For at least the reasons set forth above, Applicant respectfully requests that the Section 103 rejection of Claims 28 and 29 be withdrawn.

In view of the foregoing amendment and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully submitted,



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